ABSTRACT OF THE DISCLOSURE

~~The display RAM built into a conventional display control device uses a system in which data are sequentially written word by word, it involves a problem that, if th write speed is to be raised to match the transfer speed of display data from the microprocessor, the power consumption will increase in proportion to the transfer speed~~A display control device is designated to enable high speed writing of data into a display RAM without a substantial increase in power consumption. The width (number of bits) of write data to [[a]] the display RAM ~~in a display control device~~ is set to be an integral multiple of the width of write data supplied from an external microprocessor ~~or the like~~, and two stages of latch circuits for holding write data equivalent to one row of the display RAM are provided. A few cycles' equivalent of the write data supplied from the microprocessor ~~or the like~~ is taken into the first stage of latch circuits and, when the data are ready, they are collectively transferred to the second stage ~~of latch circuits~~, so that the data held by the second stage ~~of latch circuits~~ can be collectively transferred by a transfer gate to the display RAM for displaying.